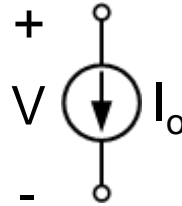


Current Mirror

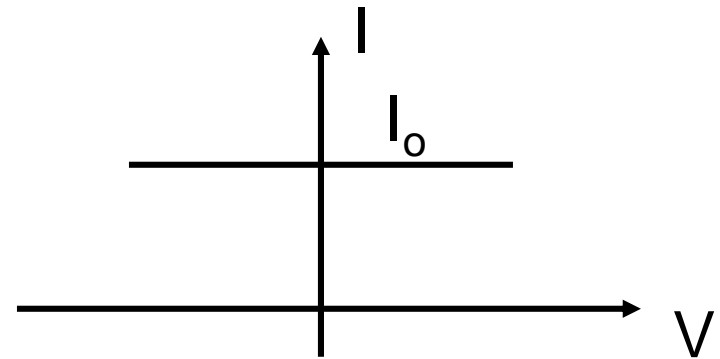
Current Source and Sink

- Symbol of current source



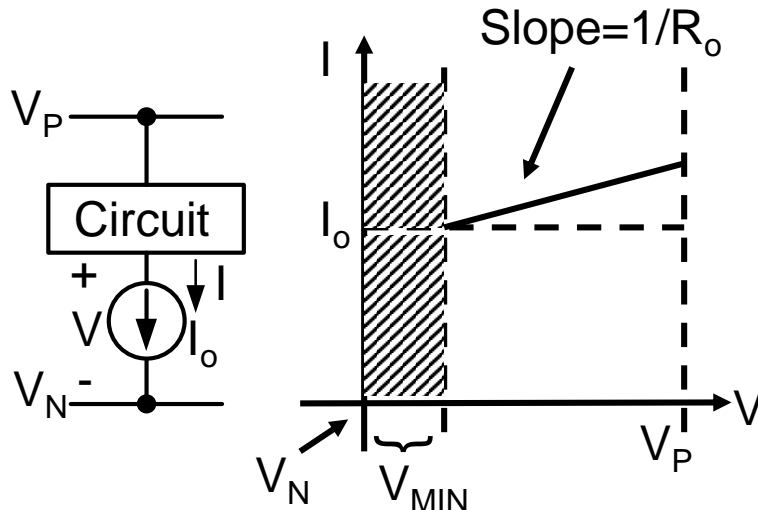
- Ideal current source

- ◆ Output resistance $\frac{\Delta V}{\Delta I} = \infty$

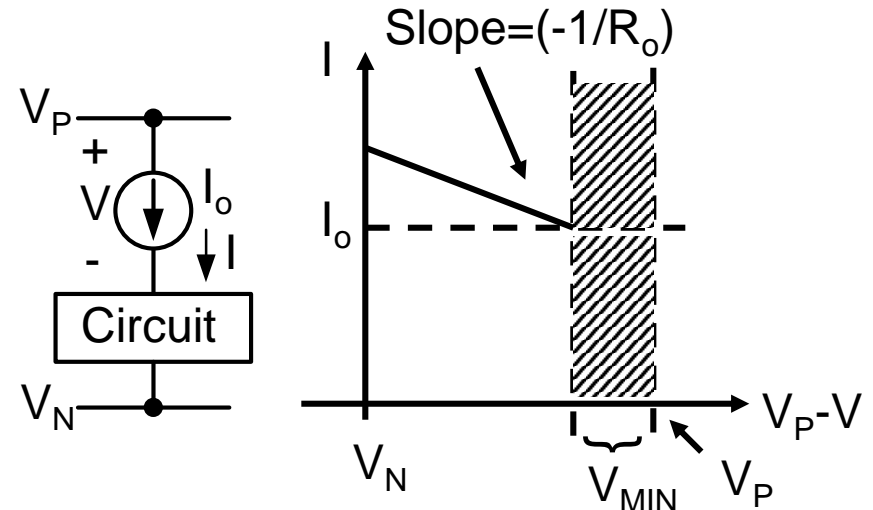


- Practical I-V characteristics

- ◆ Current sink

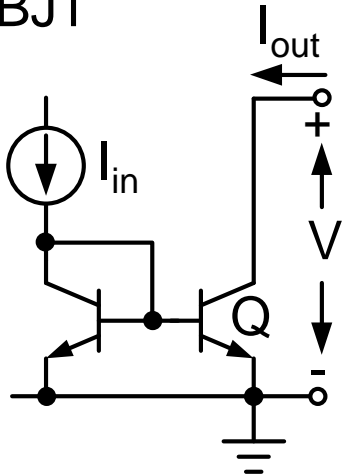


- ◆ Current source

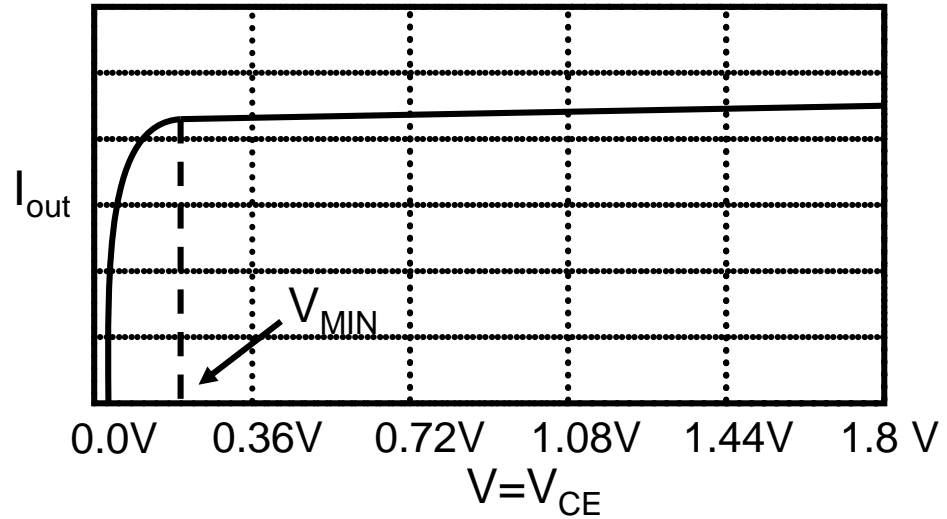


Simple Current Mirrors

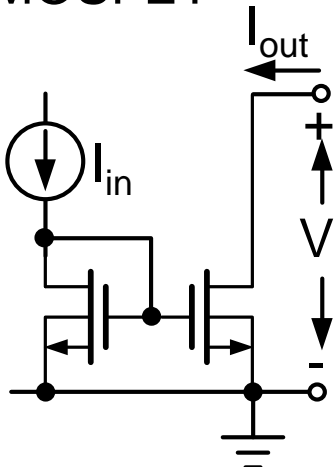
- BJT



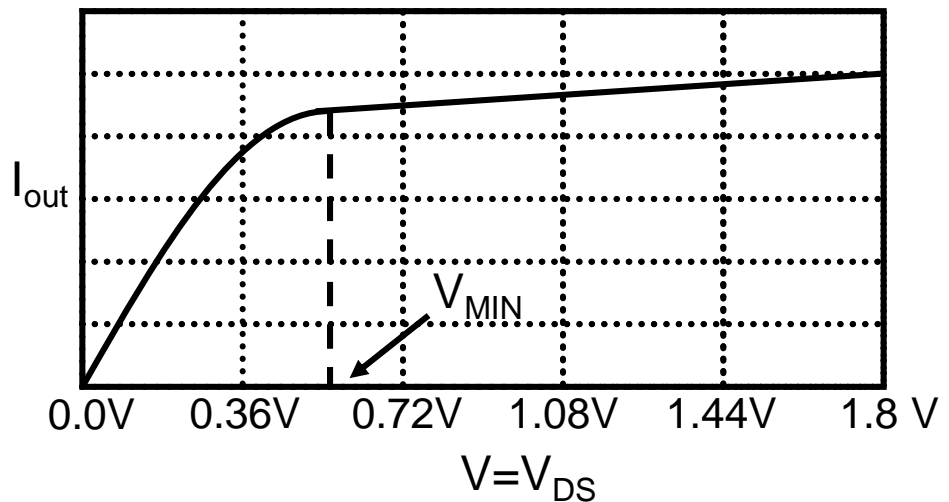
$$V_{\min} \approx V_{CE(\text{sat})}$$



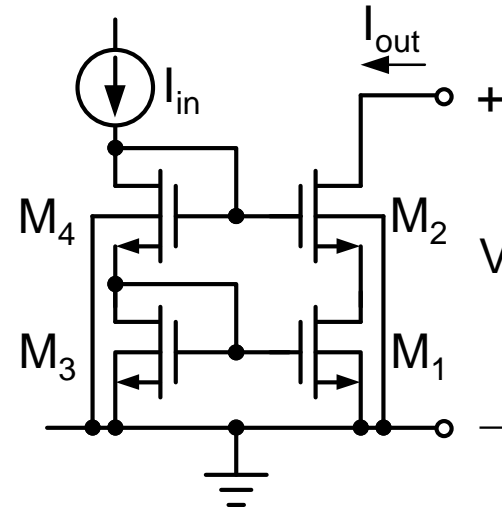
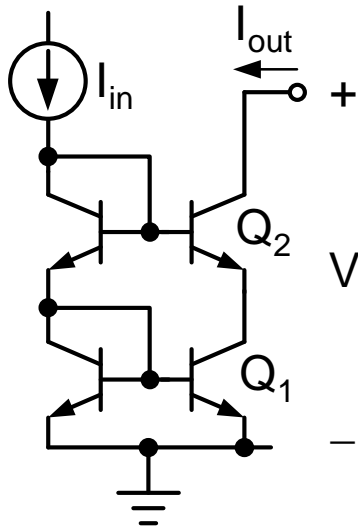
- MOSFET



$$V_{\min} \approx V_{GS} - V_T$$



Increase Output Resistance of Current Mirrors Using Cascode Structures



- Output impedance

- ◆ BJT: $R_o = r_{o2}[1+(g_{m2}+g_{o2})(r_{\pi2}/r_{o1})] \approx r_{o2}(1+g_{m2}r_{\pi2})$

- ◆ MOSFET: $R_o = r_{ds2}[1+(g_{m2}+g_{mb2}+g_{ds2})r_{ds1}] \approx \underbrace{r_{ds2}g_{m2}}_{\text{DC gain of } M_2} r_{ds1}$

- Minimum output voltage

- ◆ BJT: $V_{\min} = V_{CE1} + V_{CE2(\text{sat})} \approx V_{BE(\text{on})} + V_{CE2(\text{sat})}$

- ◆ MOSFET (assume the same size of $M_{1-4} \rightarrow$ same V_{eff}):

$$V_{g4} = V_{gs3} + V_{gs4} = 2V_{\text{eff}} + 2V_T; \quad V_{DS1} = V_{g4} - V_{gs2} = V_{\text{eff}} + V_T$$

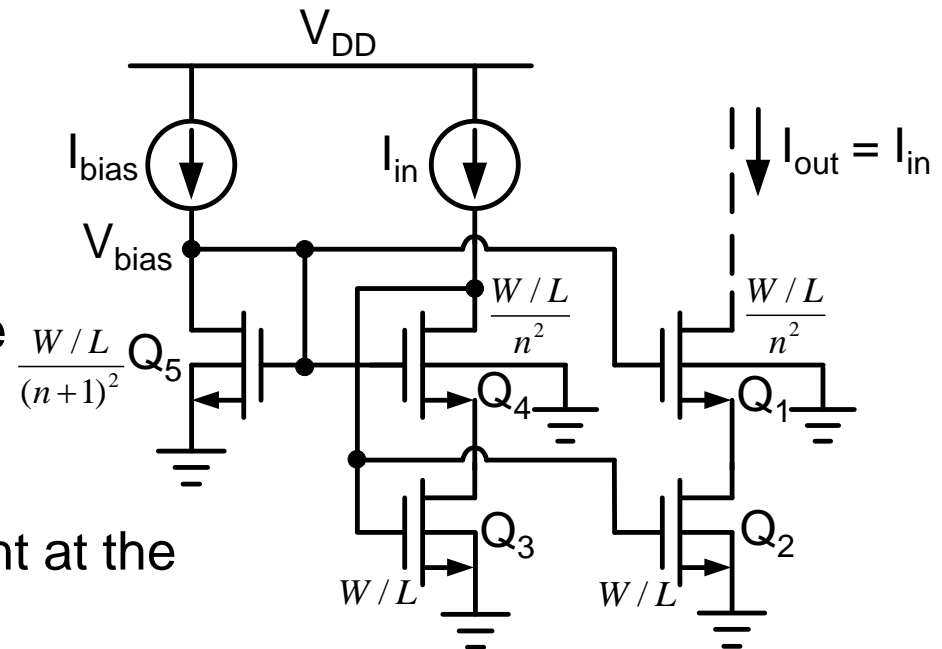
$$V_{\min} = V_{DS2(\text{sat})} + V_{DS1} = V_{\text{eff}} + (V_{\text{eff}} + V_T) = 2V_{\text{eff}} + V_T$$

Wide-Swing Current Mirrors

- $r_{ds} = 1/\lambda I$ and $L \downarrow \Rightarrow \lambda \uparrow$
- For shorter channel lengths, $L \downarrow \Rightarrow r_{ds} \downarrow \Rightarrow \text{OPAMP gain} \downarrow$
 - ◆ Cascode current mirrors can be used to increase output impedance. However, their signal swings are reduced.
 - ◆ Wide-swing cascode current mirrors are needed.

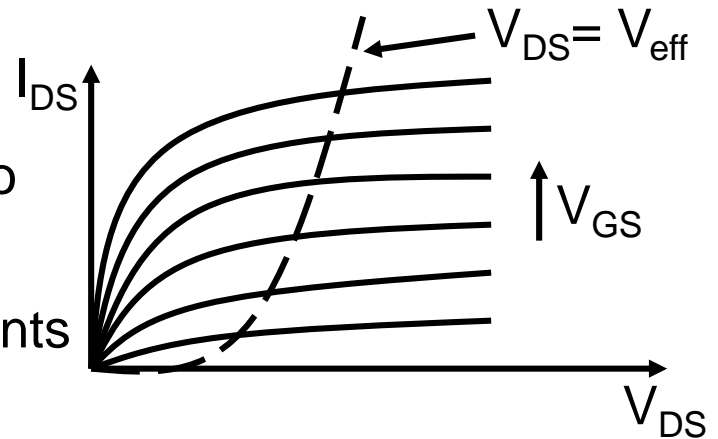
● Example

- ◆ The basic idea is to bias the drain-source voltages of transistors Q_2 and Q_3 to be close to the minimum possible without them going into the triode region.
- ◆ Q_2 and Q_3 must be biased right at the edge of the triode region.



Wide-Swing Current Mirrors (Cont.)

- ◆ Let V_{eff} be the effective transistor gate-source voltage, $V_{\text{GS}} - V_{\text{th}}$, which is also the minimum V_{DS} for a transistor to be biased in the saturation region.
- ◆ Assume all of the transistor drain currents are equal, then



$$V_{\text{eff}2} = V_{\text{eff}3} = \sqrt{\frac{2I_{\text{D}2}}{\mu_n C_{\text{ox}} (W/L)}} = V_{\text{eff}} (\because I_{\text{D}2} = \frac{\mu_n C_{\text{ox}} W}{2L} (V_{\text{GS}} - V_{\text{th}})^2)$$

$$\text{Since } \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = (n+1)^2 \left(\frac{W}{L}\right)_5 = n^2 \left(\frac{W}{L}\right)_1 = n^2 \left(\frac{W}{L}\right)_4$$

$$V_{\text{eff}1} = V_{\text{eff}4} = nV_{\text{eff}}$$

$$V_{\text{G}5} = V_{\text{G}4} = V_{\text{G}1} = (n+1)V_{\text{eff}} + V_{\text{th}}$$

$$V_{\text{D}S2} = V_{\text{D}S3} = V_{\text{G}5} - V_{\text{G}S1} = V_{\text{G}5} - (nV_{\text{eff}} + V_{\text{th}}) = V_{\text{eff}}$$

$$\Rightarrow V_{\text{out}} > V_{\text{eff}1} + V_{\text{eff}2} = (n+1)V_{\text{eff}}$$

Wide-Swing Current Mirrors (Cont.)

- ◆ A common choice: $n = 1$, $V_{out} > 2V_{eff}$
- ◆ For a safe design
 - If $I_{in} = I_{bias}$, V_{DS2} should be made a little larger ($>V_{eff}$), 0.05V to 0.1V larger depending on transistor I-V

Choose a little larger $\left(\frac{W}{L}\right)_2$ and $\left(\frac{W}{L}\right)_3$

- If I_{in} is a varying current, $I_{in} \leq I_{bias}$ must be satisfied (i.e. $V_{DS2} = V_{DS3} \geq V_{eff}$)

Constant Transconductance Bias Circuit

- Biasing circuits that provide stable transconductances

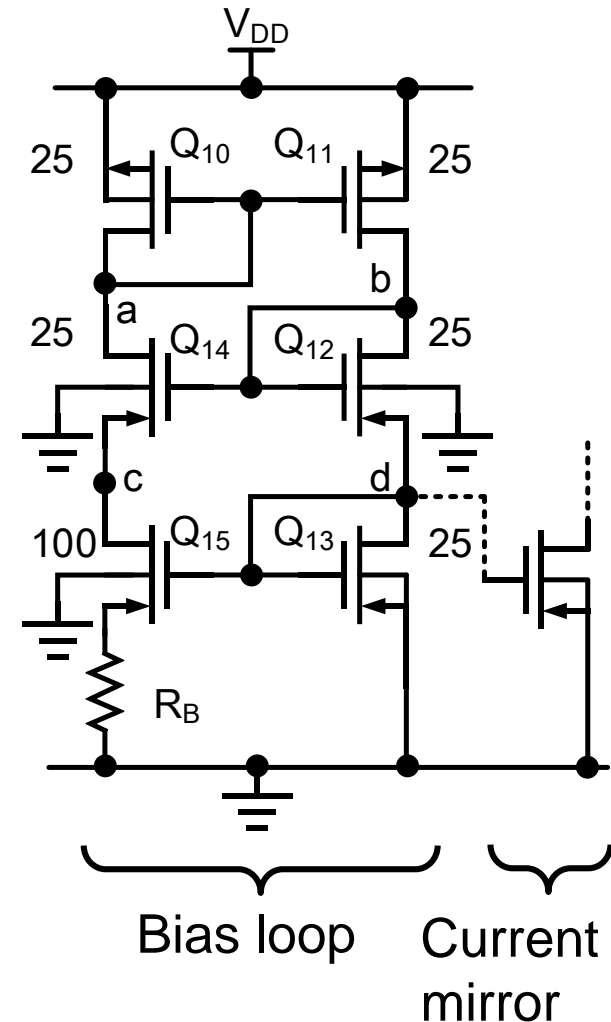
- ◆ Transistor transconductances are matched to the conductance of a resistor.

To a first-order effect, the transistor transconductances are independent of process as well as power-supply voltage and temperature variations (PVT variations).

- ◆ Q_{14} (Q_{12}) causes voltage drop between a and c (b and d) to minimize channel length modulation
- ◆ Q_{12} is diode-connected to provide a bias voltage to Q_{14}
- ◆ Example

$$\left(\frac{W}{L}\right)_{10} = \left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_{12} = \left(\frac{W}{L}\right)_{13} = \left(\frac{W}{L}\right)_{14}$$

Unity current mirror



Constant Transconductance Bias Circuit (Cont.)

$$\left\{ \begin{array}{ll} V_{\text{eff}13} = V_{\text{eff}15} + I_{D15}R_B & \text{bottom current mirror (widlar)} \\ I_{D10} = I_{D11} \text{ i. e. } I_{D13} = I_{D15} & \text{top current mirror (linear)} \\ g_{m13} = \frac{2I_{D13}}{V_{\text{eff}13}} \end{array} \right.$$

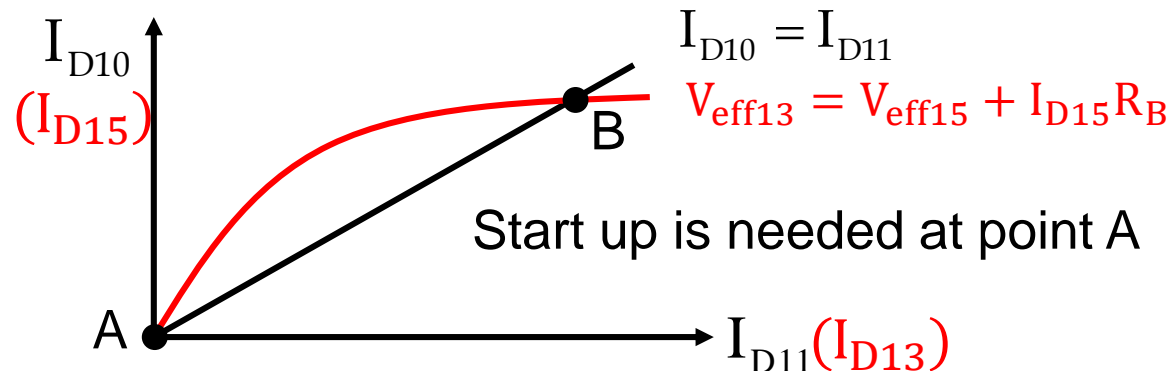
◆ Simple derivation

$$\rightarrow g_{m13} = 2 \left(\frac{V_{\text{eff}13} - V_{\text{eff}15}}{R_B} \right) \times \frac{1}{V_{\text{eff}13}} = \frac{2 \left[1 - \sqrt{\frac{(W/L)_{13}}{(W/L)_{15}}} \right]}{R_B}$$

◆ g_{m13} is determined by geometric ratios only, independent of process parameters, temperature (PVT), or any other parameters with large variability

◆ At point A, loop gain

$$= \frac{(W/L)_{11}}{(W/L)_{10}} \times \frac{(W/L)_{15}}{(W/L)_{13}}$$



Constant Transconductance Bias Circuit (Cont.)

- ◆ For a special case, $\left(\frac{W}{L}\right)_{15} = 4\left(\frac{W}{L}\right)_{13} \rightarrow g_{m13} = \frac{1}{R_B}$
- ◆ Thus, not only is g_{m13} stabilized, but all other transistors transconductances are also stabilized since the ratios of transistor currents are mainly dependent on geometry.

- ◆ For all n-channel transistors

$$g_{mi} = \sqrt{\frac{(W/L)_i I_{Di}}{(W/L)_{13} I_{D13}}} \times g_{m13}$$

- ◆ For all p-channel transistors

$$\left\{ \begin{array}{l} I_{D10} = I_{D13} \\ g_{m10} = \sqrt{2\mu_p C_{ox} (W/L)_{10} I_{D10}} \\ g_{m13} = \sqrt{2\mu_n C_{ox} (W/L)_{13} I_{D13}} \end{array} \right. \Rightarrow g_{m10} = \sqrt{\frac{\mu_p (W/L)_{10}}{\mu_n (W/L)_{13}}} \times g_{m13}$$

Similarly, $g_{mi} = \sqrt{\frac{\mu_p (W/L)_i I_{Di}}{\mu_n (W/L)_{13} I_{D13}}} \times g_{m13}$

(Larger variation due to extra $\sqrt{\mu_p/\mu_n}$ variation)

Constant Transconductance Bias Circuit (Cont.)

- P-type constant transconductance bias circuit with start-up circuit

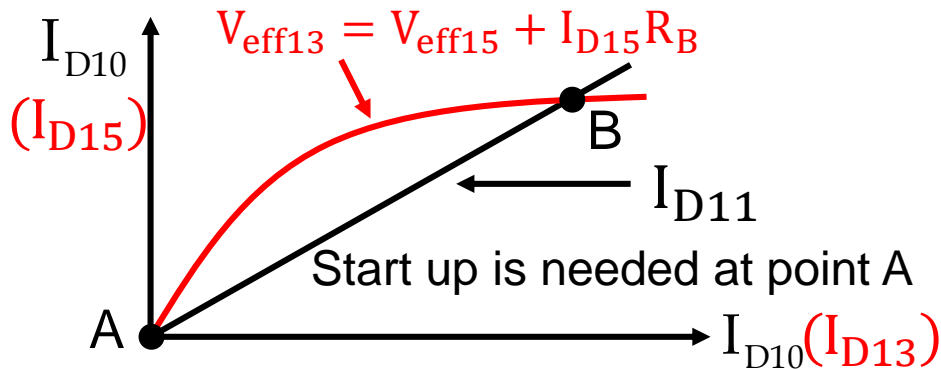
- ◆ Approximate current characteristics of the bias loop.

- ◆ Positive feedback bias loop:

- Two stable points, A and B.

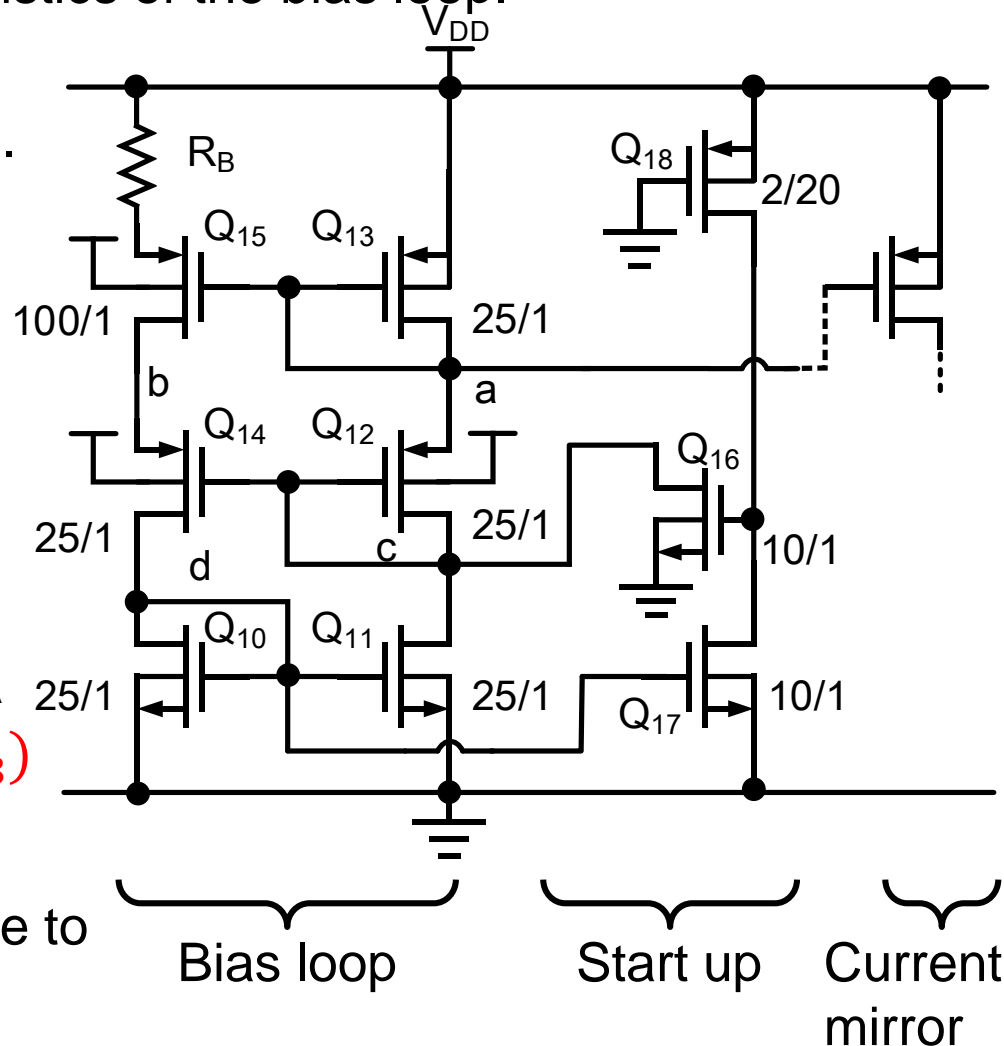
- At point A, loop gain

$$\approx \frac{(W/L)_{11}}{(W/L)_{10}} \times \frac{(W/L)_{15}}{(W/L)_{13}} = 4$$



- ◆ For all n-channel transistors

- g_{mi} has larger variation due to extra $\sqrt{\mu_n/\mu_p}$ variation



Constant Transconductance Bias Circuit (Cont.)

- Start-up circuit
 - ◆ Operational principle of start-up circuit
 - All currents in the bias loop are zero, Q_{17} will be off.
 - Q_{18} is always on, the gates of Q_{16} will be pulled high.
 - Q_{16} will inject currents into the bias loop, which will start up the circuit.
 - Once the loop starts up, Q_{17} will be on, pulling the gate of Q_{16} low, and thereby turning it off so it no longer affects the bias loop.
 - This circuit is only one example of a start-up loop, and there are many other variations.
 - For example, sometimes Q_{18} , is replaced by an actual resistor.

Constant Transconductance Bias Circuit (Cont.)

◆ Second-order effect

➤ Body effect

The equations will be slightly modified

➤ Output impedance effect

Can be reduced using cascoded p-channel current mirror

➤ Temperature effect

(i) μ is proportional to $T^{-3/2}$. This corresponds to a 27% μ reduction from 27°C(300 °k) to 100°C(373 °k)

(ii) Since $g_m = 1/R_B$ and $g_m = \mu C_{ox}(W/L)V_{eff}$

V_{eff} will be increased by 27% if temperature effect of R_B is ignored. (positive TC of R_B , if it is on-chip, can somewhat offset this increase)

(iii) As long as V_{eff} has not been designed to be too large (or V_{DD} is large enough), this limitation is tolerable in most applications.

Widlar Current Sources

- For large current mirror ratio

- ◆ Bipolar

$$I_{REF} = 0.73\text{mA}, R_A = 5\text{k}\Omega$$

$$V_{BE1} - V_{BE2} = I_{C2} R_A$$

$$\Rightarrow V_T \ln \frac{I_{REF}}{I_{C2}} = I_{C2} R_A$$

⇒ Trial and error to determine I_{C2}

$$\Rightarrow I_{C2} = 19\mu\text{A}$$

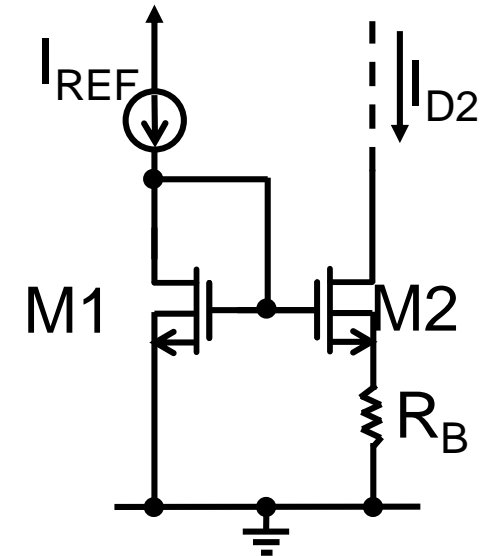
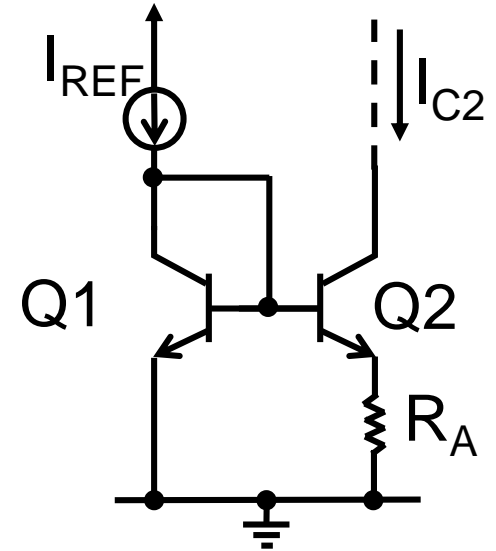
- ◆ MOSFET

$$V_{eff1} = V_{eff2} + I_{D2} \times R_B$$

$$\text{Assume } I_D = K \cdot V_{eff}^2 \Rightarrow \sqrt{\frac{I_{REF}}{K}} = \sqrt{\frac{I_{D2}}{K}} + (\sqrt{I_{D2}})^2 \times R_B$$

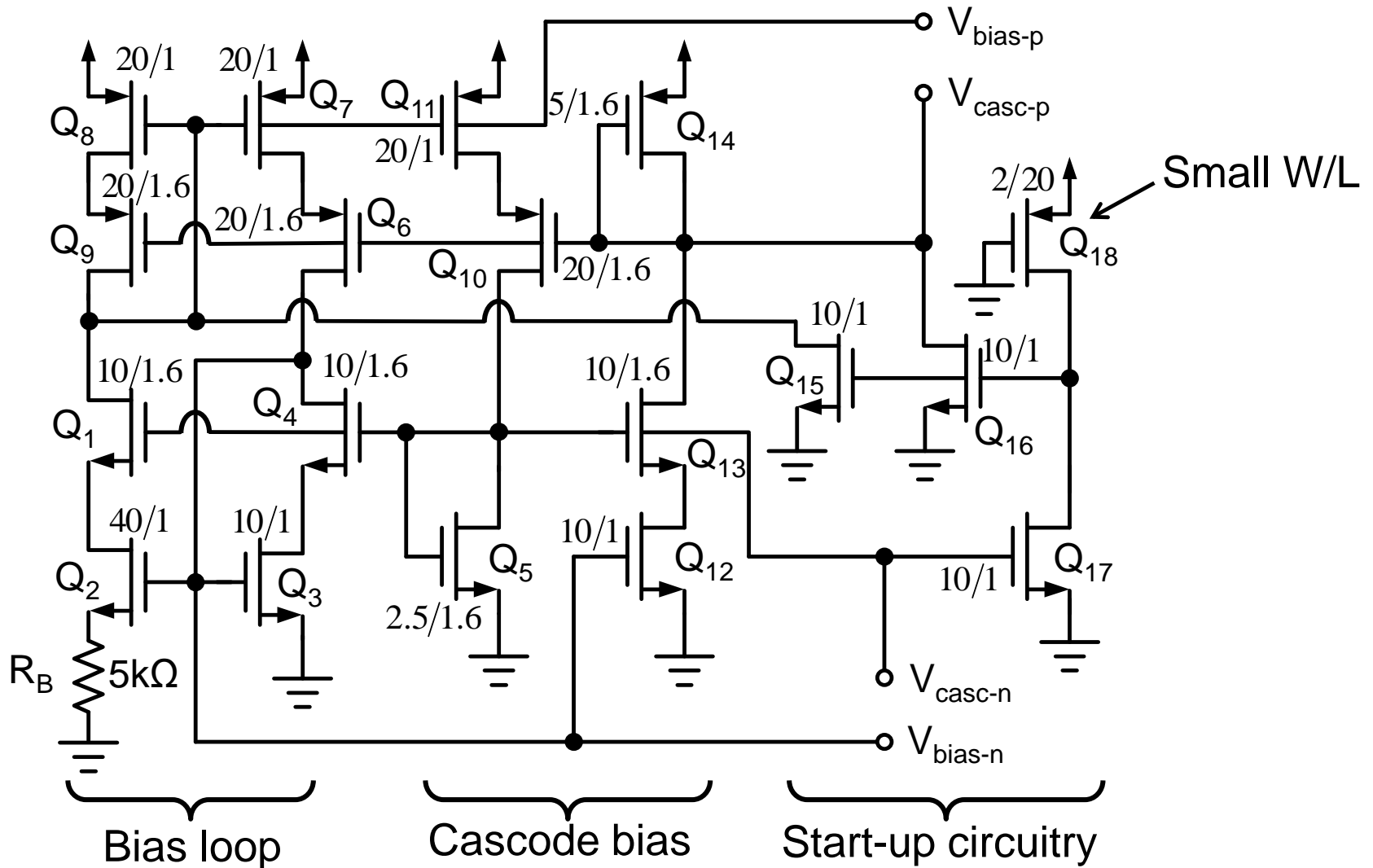
$$\sqrt{I_{D2}} = \frac{-\sqrt{\frac{1}{K}} \pm \sqrt{\frac{1}{K} + 4R_B \sqrt{\frac{I_{REF}}{K}}}}{2R_B} > 0$$

$$\Rightarrow I_{D2} = \frac{1 + 2R_B \sqrt{KI_{REF}} - \sqrt{1 + 4R_B \sqrt{KI_{REF}}}}{2K(R_B)^2}$$



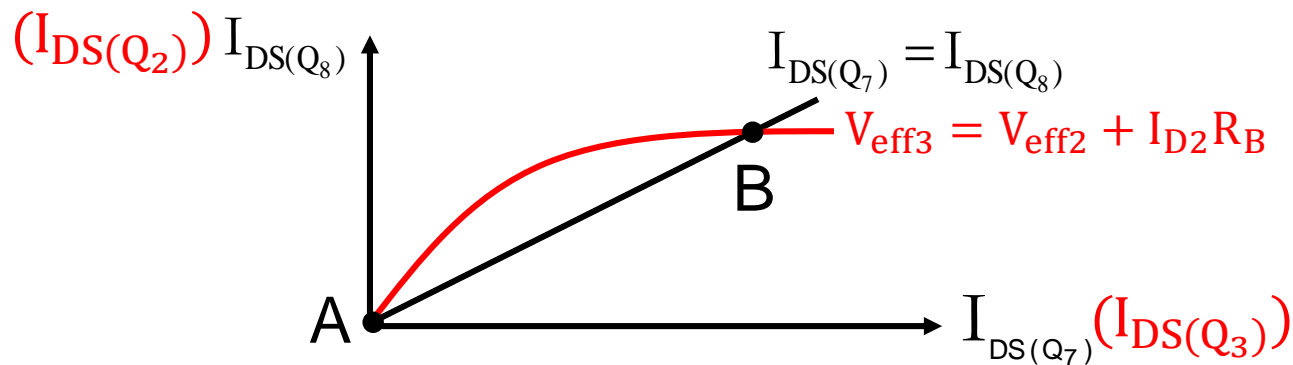
Wide-Swing Constant Transconductance Bias Circuit

- Wide-swing current mirrors + constant g_m bias circuit



Wide-Swing Constant Transconductance Bias Circuit (Cont.)

- ◆ Wide-swing :
 - Minimize V_{DS} of bias transistors to V_{eff}
- ◆ Constant g_m : $g_m = 1/R_B$
- ◆ Minimization of finite output impedance effect :
 - Use cascode bias
- ◆ Start-up
 - Approximate current characteristics of the bias loop
 - At point A, loop gain $\approx \frac{(W/L)_7}{(W/L)_8} \bullet \frac{(W/L)_2}{(W/L)_3} = 4$



Wide-Swing Constant Transconductance Bias Circuit (Cont.)

- ◆ Start-up (Cont.)
 - Positive feedback bias loop:
Two stable points, A and B.
At point A, loop gain > 1 must be satisfied.
- ◆ Operational principle of start-up circuit
 - All currents in the bias loop are zero, Q_{17} will be off
 - Q_{18} is always on, the gates of Q_{15} and Q_{16} will be pulled high
 - Q_{15} and Q_{16} will inject currents into the bias loop, which will start up the circuit.
 - Once the loop starts up, Q_{17} will be on, pulling the gates of Q_{15} and Q_{16} low, and thereby turning them off so they no longer affect the bias loop.
- ◆ This circuit is only one example of a start-up loop, and there are many other variations.
 - For example, sometimes Q_{18} , is replaced by an actual resistor

Enhanced-Output-Impedance Current Mirrors

- General structure

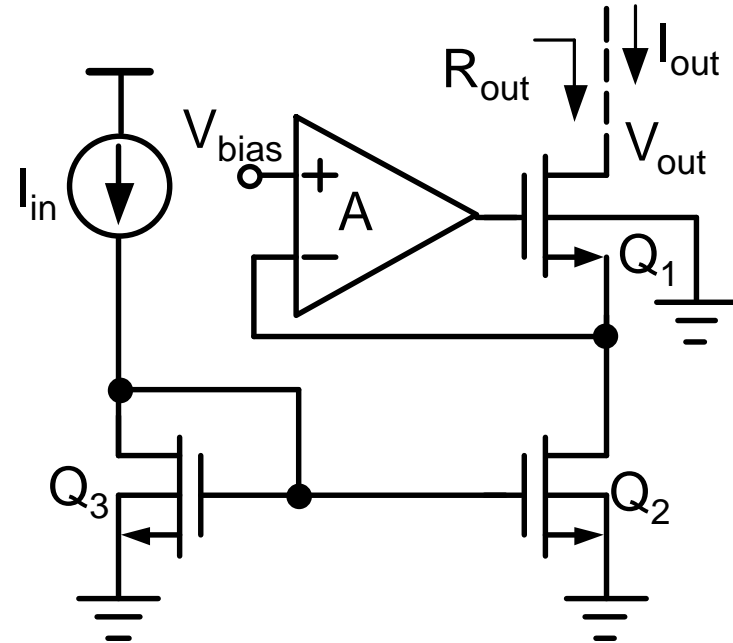
- ◆ For wide-swing, $V_{\text{bias}} \approx V_{\text{eff}2}$

- ◆ $R_{\text{out}} \approx g_{m1} r_{ds1} r_{ds2} (1+A)$

- ◆ This technique for output-impedance enhancement is not useful when bipolar Transistors (Q_1 , Q_2 , and Q_3) are used.

- ◆ R_{out} might be limited by R_{db} .

- This parasitic conductance, R_{db} , is a result of collisions between highly energized electrons resulting in electron-hole pairs to be generated with the holes escaping to the substrate. The generation of these electron-hole pairs is commonly called impact ionization.



Enhanced-Output-Impedance Current Mirrors (Cont.)

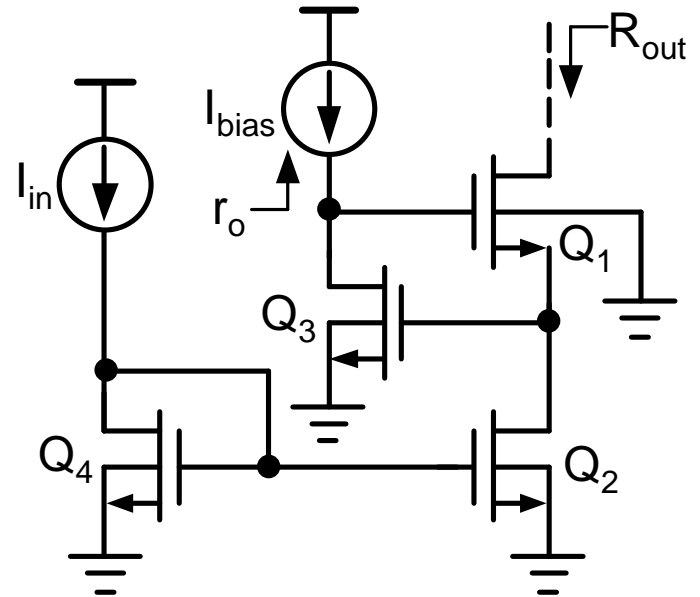
- A simple implementation example : regulated cascode mirror

$$R_{out} \cong g_{m1} r_{ds1} r_{ds2} [1 + g_{m3} (r_{ds3} \parallel r_o)]$$

$$\text{where } r_{ds3} \parallel r_o \approx \frac{r_{ds3}}{2}$$

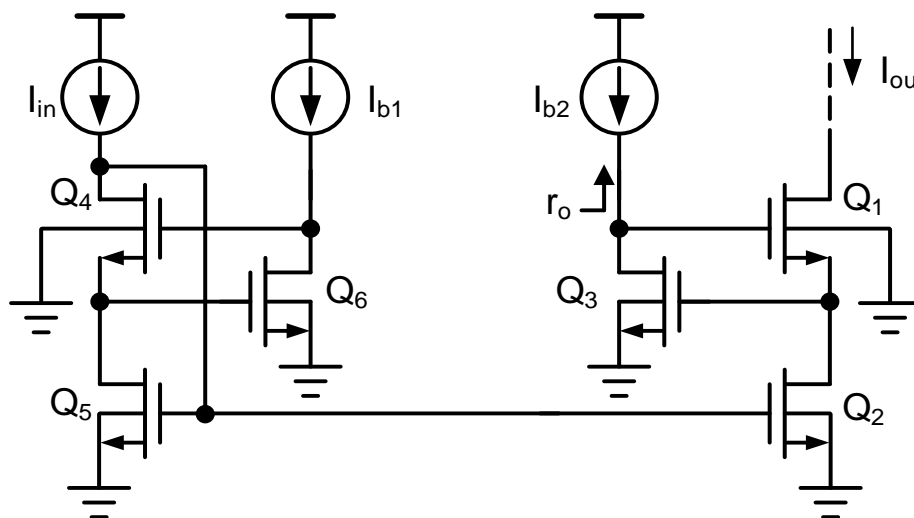
It is not useful when bipolar transistors are used.

$$V_{ds2} = V_{eff3} + V_{th} \text{ (not a wide-swing source)}$$



Enhanced-Output-Impedance Current Mirrors (Cont.)

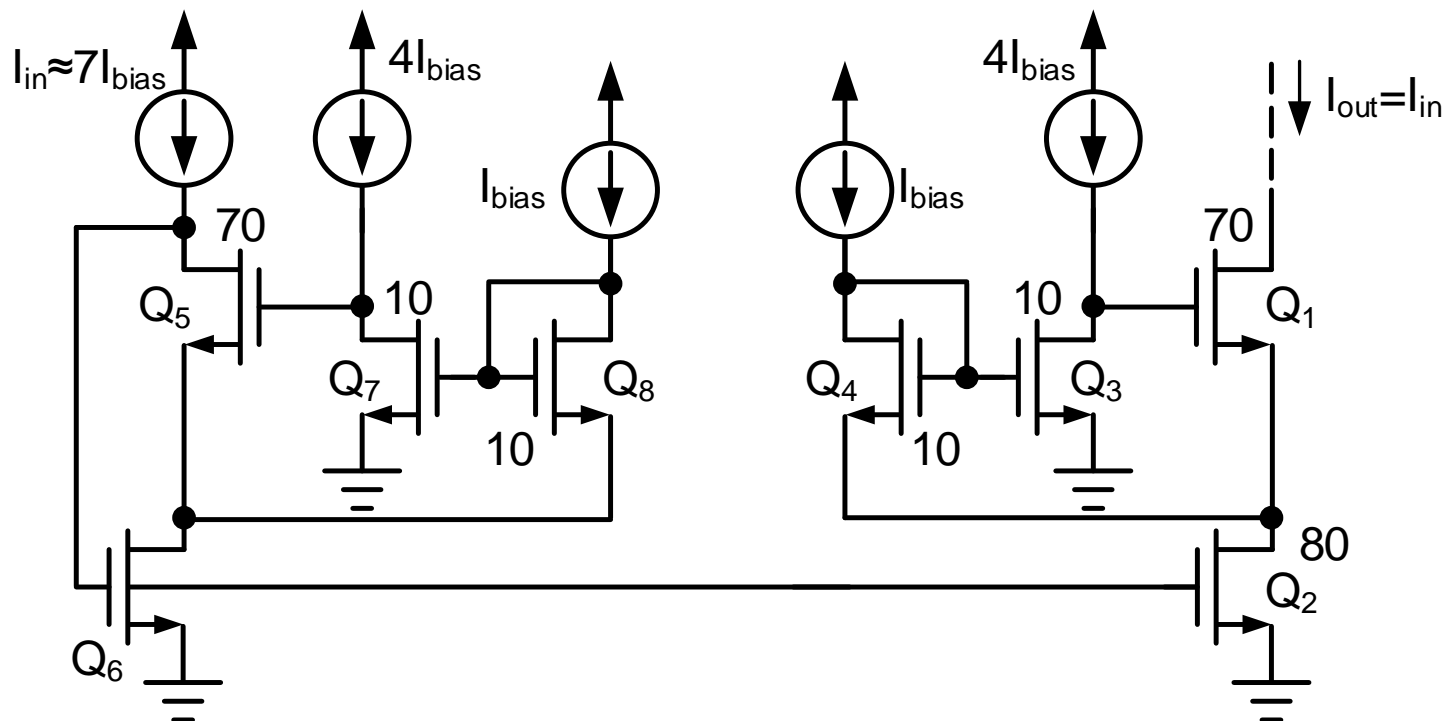
- Sackinger implementation



- ◆ Use regulated cascode to increase output impedance
- ◆ $R_{out} \cong g_{m1} r_{ds1} r_{ds2} [1 + g_{m3} (r_{ds3} \parallel r_o)]$ where $r_{ds3} \parallel r_o \approx \frac{r_{ds3}}{2}$
- ◆ $Q_1, Q_2, Q_3, I_{B1}, I_{out}$ match $Q_4, Q_5, Q_6, I_{B2}, I_{in}$, respectively.
- ◆ $V_{DS2} = V_{DS5} = V_{eff3} + V_{tn}$ rather than the minimum required, which could be equal to V_{eff2} . This limitation is especially harmful for modern technologies operating with power voltages of 1V or lower.

Enhanced-Output-Impedance Current Mirrors (Cont.)

- Wide-swing + enhance output-impedance current mirrors



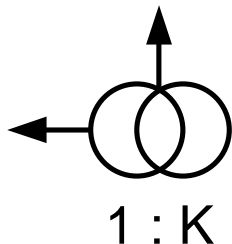
- ◆ Level shift in front of the common source amplifier in the regulated cascode current source

Enhanced-Output-Impedance Current Mirrors (Cont.)

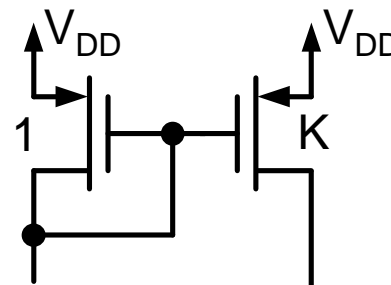
- ◆ All transistors are biased with nearly the same current density, except for Q_3 and Q_7 . As a result, all transistors have the same effective gate-source voltage, V_{eff} , except for Q_3 and Q_7 , which have gate-source voltage of $2V_{\text{eff}}$ because they are biased at four times the current density.
- ◆ $V_{G3} = 2V_{\text{eff}} + V_{\text{tn}}$
- ◆ $V_{\text{DS}2} = V_{\text{S}4} = V_{G3} - V_{\text{GS}4} = (2V_{\text{eff}} + V_{\text{tn}}) - (V_{\text{eff}} + V_{\text{tn}}) = V_{\text{eff}}$
- ◆ $V_{\text{out}} > V_{\text{DS}2} + V_{\text{eff}1} = 2V_{\text{eff}}$

Current Mirror Symbol

- Symbol



- A circuit example



Increase Output Resistance of Current Mirrors Using Emitter/Source-Degenerated Structures

- Large R_o of current source/sink => more like ideal current source/sink

- For MOSFET

$$R_o = \frac{1}{\lambda I_o}$$

$$I = \frac{1}{2} K' \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

- For BJT

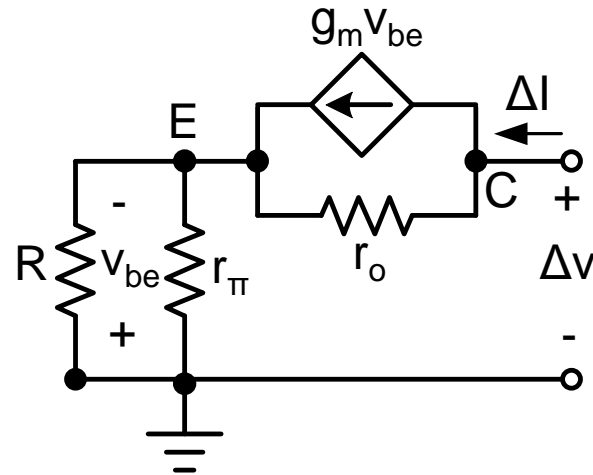
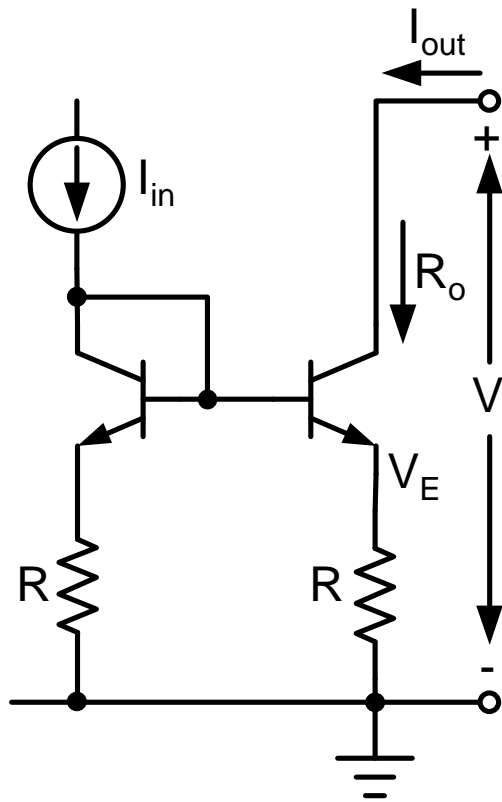
$$R_o = \frac{V_{AF}}{I_C}$$

$$I_C = I_S (1 - e^{-V_{BE}/V_I}) (1 + V_{CE}/V_{AF})$$

- Negative feedback to increase R_o
 - ◆ Emitter-Degenerated
 - ◆ Source-Degenerated

Increase Output Resistance of Current Mirrors Using Emitter/Source-Degenerated Structures (Cont.)

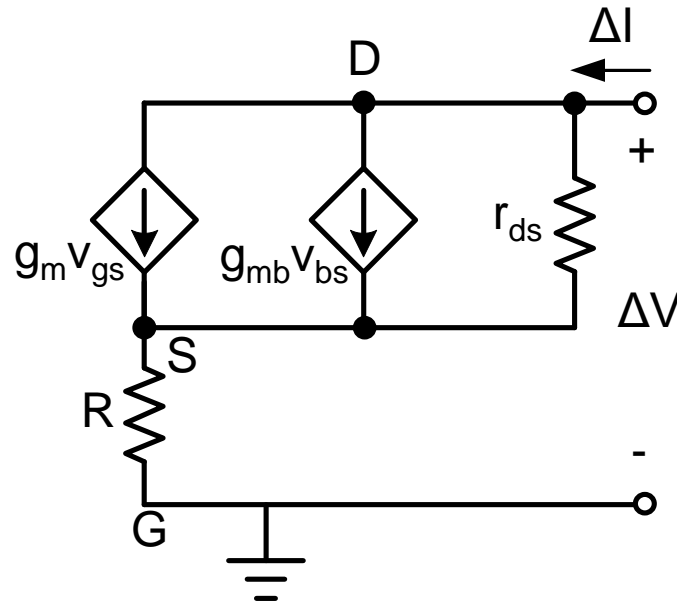
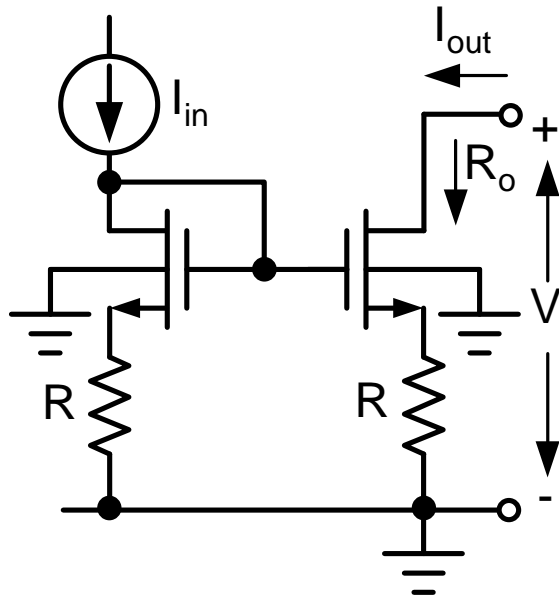
- Emitter-Degenerated



$$\begin{aligned}
 \Delta V &= \Delta I(r_\pi // R) + [\Delta I + g_m \Delta I(r_\pi // R)]r_o \\
 &= \Delta I r_o \left[\frac{1}{r_o} (r_\pi // R) + 1 + g_m (r_\pi // R) \right] \\
 &= \Delta I r_o [1 + (g_m + g_o)(r_\pi // R)] \\
 R_o &= \frac{\Delta V}{\Delta I} = r_o [1 + (g_m + g_o)(r_\pi // R)] \\
 &\approx r_o [1 + g_m (r_\pi // R)]
 \end{aligned}$$

Increase Output Resistance of Current Mirrors Using Emitter/Source-Degenerated Structures (Cont.)

- Source-Degenerated



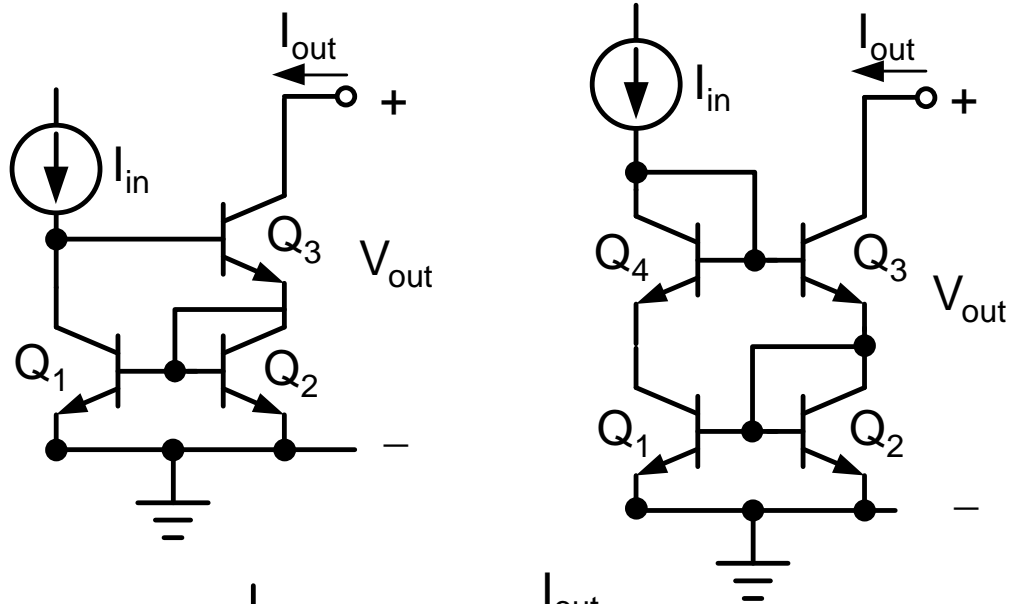
Similarly,
$$R_o = \frac{\Delta V}{\Delta I} = r_{ds} [1 + (g_m + g_{mb} + g_{ds})R] \approx r_{ds} (1 + g_m R)$$

Increase Ro Using Wilson Current Mirror

● BJT

$$I_{out} = I_{in} \left(1 - \frac{2}{\beta_F^2 + \beta_F + 1} \right)$$

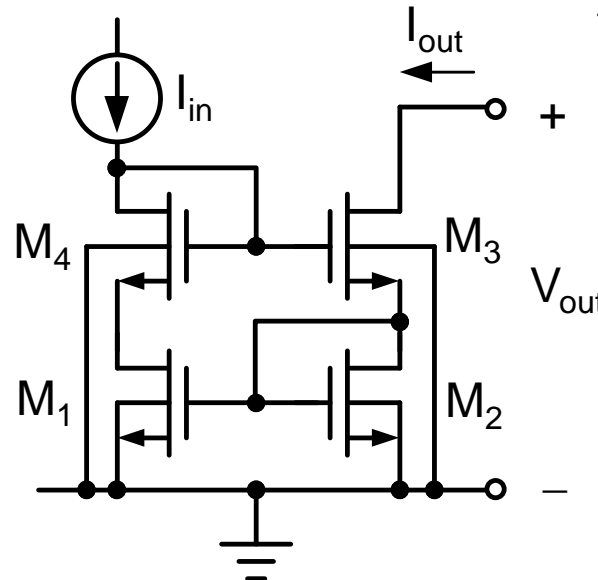
$$r_{out} \approx \frac{r_{o3} \beta_{F3}}{2}$$



● MOSFET

$$r_{out} = r_{ds3} g_{m3} (r_{ds1} // r_{in})$$

$$\approx g_{m3} r_{ds1} r_{ds3}$$

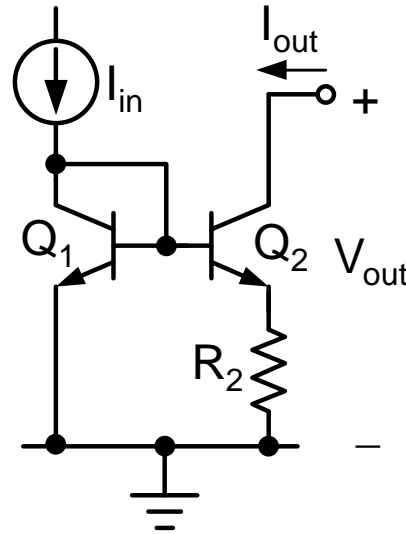


Increase R_o Using Widlar Current Mirror (Cont.)

- Large area ratio caused by large current ratio is reduced

$$V_{BE1} - V_{BE2} = I_{C2} R_2$$

$$V_t \ln(I_{in}/I_{C2}) = I_{C2} R_2$$



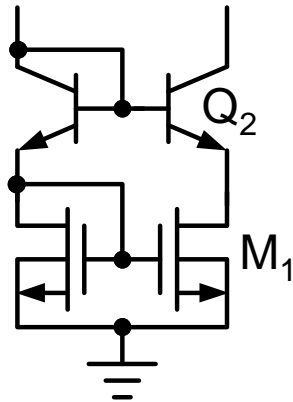
- Iterative method to obtain the value of I_{C2}

$$r_{out} = r_{o2}(1 + g_{m2} R_2)$$

(For CMOS implementation, Q_1 and Q_2 are NMOS)

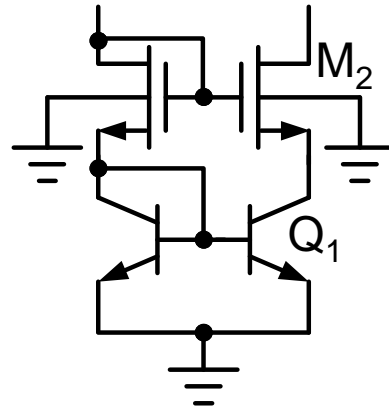
BiCMOS Cascode Current Mirrors

- BiCMOS



$$R_o = \beta r_{o2}$$

(same as bipolar cascode)



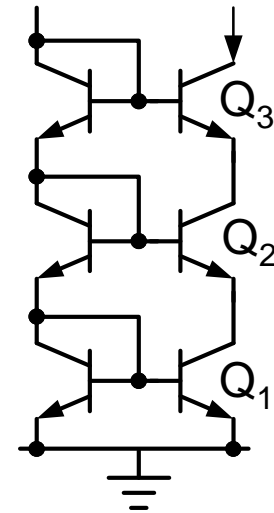
$$R_o = g_{m2} r_{o2} r_{o1} = 10\text{M}\Omega$$

- ◆ $V_o > V_{BE} + V_{CE(\text{sat})}$ (BJT)
- ◆ $V_o > V_{gs} + V_{DS(\text{sat})}$ (MOSFET)
- ◆ $V_o > V_{gs} + V_{CE(\text{sat})}$ (BiCMOS)
- ◆ $R_{o(\text{BiCMOS})} \approx R_{o(\text{BJT})} > R_{o(\text{CMOS})}$

BiCMOS Double Cascode Current Mirrors

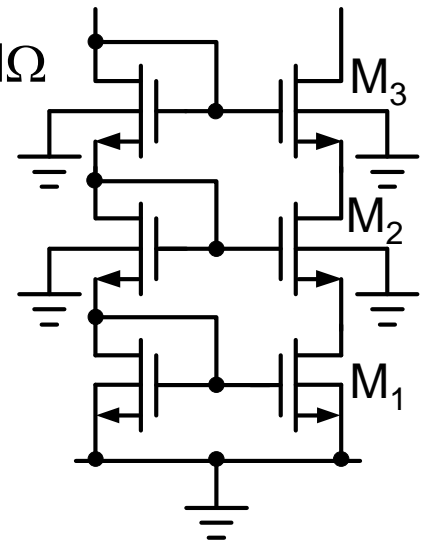
● BJT

- ◆ For $\beta=100$, $V_A=50V$, $I_o=100\mu A$, $\beta r_{o3}=50M\Omega$
 - $R_o = \beta r_{o3}$
 - No improvement from cascode
 - $V_o > 2V_{BE} + V_{CE(sat)} = V_{min}$



● MOSFET

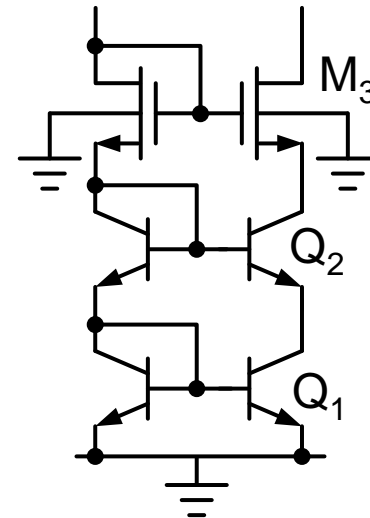
- ◆ For $(W/L)_2=5$, $\mu_n C_{ox}=40\mu A/V^2$, $\lambda=0.1V^{-1}$, $g_m r_{o2}=2M\Omega$
 - $R_o = (g_{m3} r_{o3})(g_{m2} r_{o2}) r_{o1}$
 - With same parameter as before
 - $R_o = 40M\Omega$
 - $V_o > 2V_{GS} + V_{DS(sat)} = V_{min}$



BiCMOS Double Cascode Current Mirrors (Cont.)

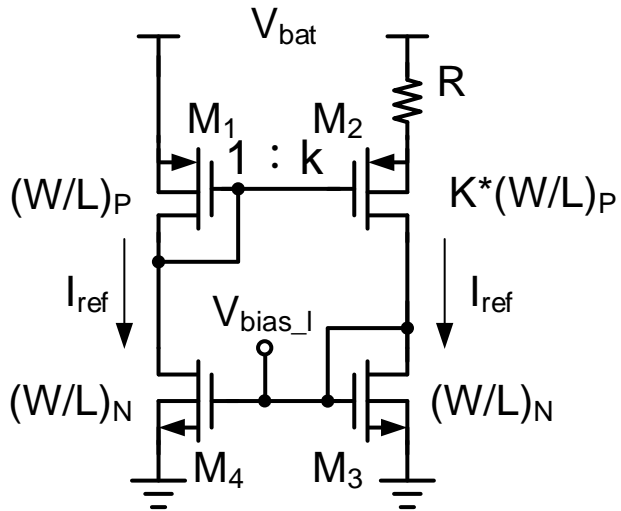
- BiCMOS

- ◆ $R_o = (g_{m3} r_{o3}) \beta r_{o2} = 1000 M\Omega$
- ◆ Practical limit : stray conductance
- ◆ $V_o > 2V_{BE} + V_{DS(sat)} = V_{min}$



- The highest R_o can be realized by using BiCMOS or CMOS. However, $R_{o(\text{BiCMOS})} > R_{o(\text{CMOS})}$ & $V_{min(\text{BiCMOS})} < V_{min(\text{CMOS})}$. (\because In general, $V_{gs} > V_{BE}$) BiCMOS provides larger voltage swing.

Stability of Constant gm Bias



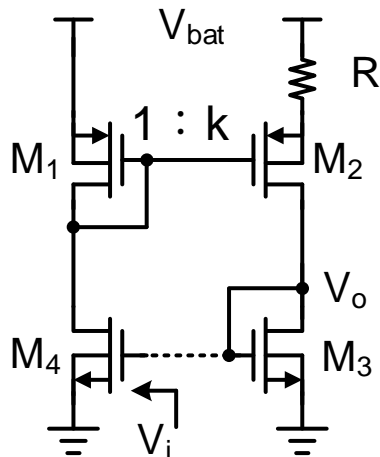
$$V_{SG1} = V_{SG2} + I_{ref} \times R$$

$$\Rightarrow I_{ref} = \frac{2}{\mu_p C_{OX} (W/L)_P} \cdot \frac{1}{R^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2 \text{ or } 0$$

$$\Rightarrow g_{m1} = \sqrt{2\mu_p C_{OX} (W/L)_P \cdot I_{ref}}$$

$$\Rightarrow g_{m1} = \frac{1}{R} \Rightarrow g_{m2} = \frac{\sqrt{K}}{R}$$

● DC loop gain, A_0



$$A_0 = -g_{m4} \times \left(\frac{1}{g_{m1}}\right) \times \left(-\frac{g_{m2}}{1 + g_{m2}R}\right) \times \left(\frac{1}{g_{m3}}\right)$$

$$= g_{m4} \times \left(\frac{1}{g_{m1}}\right) \times \left(\frac{g_{m2}}{1 + g_{m2}R}\right) \times \left(\frac{1}{g_{m3}}\right)$$

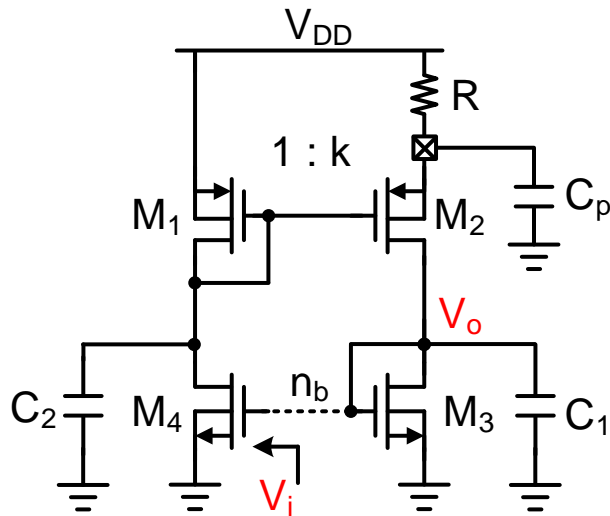
→ positive feedback

$$= (R) \times \left(\frac{\sqrt{K}/R}{1 + (\sqrt{K}/R) \cdot R}\right) = \frac{\sqrt{K}}{1 + \sqrt{K}} < 1$$

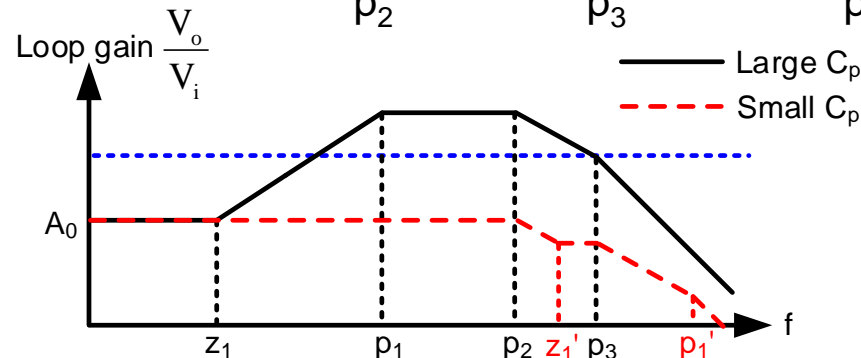
→ stable at DC

Stability of Constant gm Bias (Cont.)

- AC voltage loop gain



$$\frac{V_o}{V_i} \approx \left(\frac{g_{m4}}{g_{m1}} \cdot \frac{g_{m2}}{g_{m3}} \right) \frac{\overbrace{sRC_p + 1}^{z_1}}{\underbrace{(sC_1/g_{m3} + 1)}_{p_2} \underbrace{(sC_2/g_{m1} + 1)}_{p_3} \underbrace{(sRC_p + g_{m2}R + 1)}_{p_1}}$$



- With large $C_p \rightarrow$ positive feedback loop and loop gain $> 1 \rightarrow$ Unstable
- Pole-zero pair induced by C_p and R
 - ω_{z1} is always less than ω_{p1} : $\omega_{p1}/\omega_{z1} = 1 + g_{m2}R = 1 + \sqrt{k}$
 - $\omega_{p1} \leq \omega_{p2}$ and $\omega_{p1} \leq \omega_{p3} \rightarrow$ loop gain $> 1 \rightarrow$ the bias circuit unstable
- Solution: Add an on-chip capacitor at node n_b , such that $\omega_{p2} \leq \omega_{z1}$

$$\omega_{p2} \leq \omega_{z1} \Rightarrow \frac{g_{m3}}{C_1} \leq \frac{1}{RC_p} \Rightarrow C_1 \geq g_{m3}RC_p = \sqrt{\frac{\mu_n C_{oxn} (W/L)_{M3}}{\mu_p C_{oxp} (W/L)_{M1}}} C_p$$

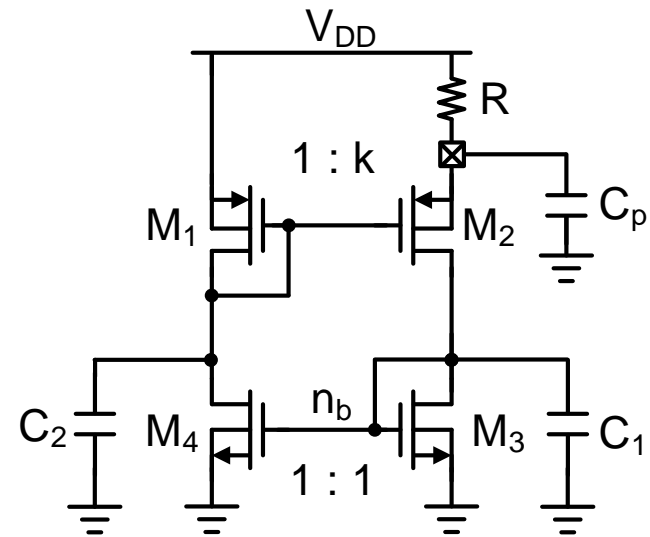
Stability compensation criteria

- Furthermore, $C1 \nearrow \rightarrow$ PSRR \nearrow

Example: Stability Compensation of Constant gm Bias

- Constant gm bias circuit
 - ◆ T-like 0.18 μm process
 - ◆ Parameter

g_{m1}	53.5 μS	R	20k Ω
g_{m2}	96.3 μS	C_p	3pF
$g_{m3,4}$	88 μS	C_1	46fF
I_{bias}	7.2 μA	C_2	135fF



- Stability of bias circuit

- ◆ $\omega_{p1} = \frac{1 + g_{m2}R}{RC_p} \approx 2\pi \times 7.76\text{MHz}$, $\omega_{p2} = \frac{g_{m3}}{C_1} \approx 2\pi \times 304.5\text{MHz}$, $\omega_{p3} = \frac{g_{m1}}{C_2} \approx 2\pi \times 63.1\text{MHz}$
- ◆ $\omega_{p1} < \omega_{p2}$ and $\omega_{p1} < \omega_{p3} \rightarrow$ unstable

- Stability compensation

- ◆ Add an on-chip capacitor at node n_b such that $\omega_{p2} < \omega_{z1}$

$$C_1 \geq g_{m3}RC_p = 1.76C_p = 5.28\text{pF}$$

$$\frac{V_o}{V_i} \approx \left(\frac{g_{m2}g_{m4}}{g_{m1}g_{m3}} \right) \frac{sRC_p + 1}{(sC_1/g_{m3} + 1)(sC_2/g_{m1} + 1)(sRC_p + g_{m2}R + 1)}$$